A novel approach for improving gate-stack reliability

12 January 2021, by Jacopo Franco, Jean-François de Marneffe

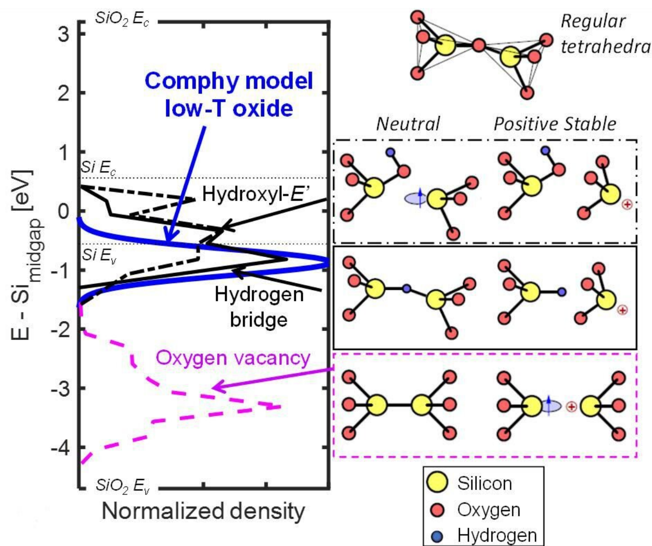

Figure 1: (Left) Comparison of the calculated energy levels of known SiO2 defect structures with the trap energy levels as estimated by modelling with Comphy the electrical NBTI data. The best match is the Hydroxyl-E' defect; other often-blamed defect candidates such as the oxygen vacancy are instead ruled out. (Right) Atomic configurations of the different defect structures. Credit: imec

Bias temperature instability (BTI) is a well-known aging mechanism in metal-oxide-semiconductor field-effect transistors (MOSFETs), which can severely affect the device performance and reliability. It typically manifests itself as an undesirable progressive increase of the device threshold voltage and a decrease of the drain current. BTI is ascribed to the presence of defects in the gate dielectrics and at the interface with the Si channel, which can trap charge carriers from the device conduction channel.

For n-type devices operating at positive on-state gate voltage, electron traps in the high-k dielectric are the primary concern. A nanometer-thin interfacial layer of native Si oxide (SiO_2) is used in current high-k/metal-gate technology to act—thanks to its large bandgap—as a tunneling barrier to reduce electron trapping and improve the PBTI ("Positive' BTI) reliability.

In p-type devices, instead, hole traps in the SiO_2 interfacial layer itself and interface defects are responsible for NBTI ("Negative' BTI). Traditionally, SiO_2 has been grown at elevated temperatures (~1000+ °C), and or exposed to similar high temperatures during the source/drain doping activation anneal in the so-called 'gate-first' integration flow. This resulted in an excellent SiO_2 layer quality, with negligible defectivity. To enable the use of various gate metals, as of the ~32nm node industry has moved to the so-called 'replacement gate' integration flow in which the final gate stack is deposited only after the doping activation anneal. For this by-now industry-standard flow, fast 'reliability anneals' (~900°C) are customary to make sure the dielectric stack is still exposed to the high temperature required to reduce its defectivity.

But what if thermal budget is restricted?

Recently, sequential 3-D integration has been proposed as a new chip manufacturing concept to further extend Moore's Law. This approach consists of stacking on top of each other multiple sequentially processed device layers (or tiers). For the fabrication of upper tiers, high-temperature (>600°C) steps are not allowed as they would degrade the transistors and interconnects already residing in the bottom tier. Such thermal budget limitation opens up new challenges for device fabrication, including the gate stack optimization for sufficient device reliability. When not grown at or exposed to elevated temperatures, SiO_2 itself contains a large density of hole trap defects, which is particularly detrimental for the NBTI reliability.

The research team at imec, in collaboration with

Vienna University of Technology (Prof. Tibor Grasser's group) and K.U. Leuven (Prof. V. Afanas'ev and Prof. A. Stesmans), has developed a novel process that significantly improves the quality of SiO_2 layers grown at reduced temperatures, and therefore enables excellent NBTI reliability of pMOS devices without requiring a high temperature anneal. The development is based on the fundamental understanding of the microscopic nature, the formation mechanism and the electrical behavior of defects in SiO_2.

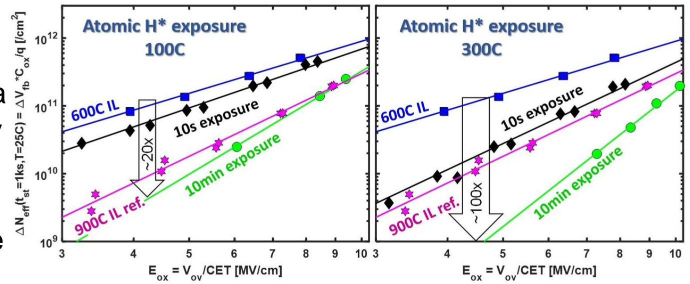

Figure 2 – Impact of the atomic H* treatment on the hole trap defect density within a 600°C grown SiO2 layer (left) after exposure at 100°C and (right) after exposure at 300°C. A high-quality 900°C layer is also shown as a reference. Credit: imec

Unveiling the hole traps in (low-temperature) SiO_2

The first step to find a low thermal budget solution for NBTI reliability was to identify the responsible defects. The team has therefore studied the electrical NBTI signature of defects in low-temperature SiO_2 using the Comphy modeling framework (developed in collaboration with the group of Prof. Tibor Grasser at Vienna University of Technology, which also co-authored this work). The estimated energy level of the hole traps within the SiO_2 bandgap were then compared with those obtained from ab-initio calculations of known SiO_2 defect structures.

From this preliminary study, the hydroxyl-E' center—an SiO_2 defect where a Si-O-Si bond structure converts into a Si-O-H structure—was identified as the most likely defect candidate. This defect preferentially forms at stretched Si-O-Si bonds, which are present due to the mechanical strain arising from the lattice mismatch between Si and SiO_2. If one interstitial hydrogen atom gets nearby a stretched Si-O-Si site during the fabrication process, it tends to form a bond with the O atom (Si-O-H), leaving behind an unsaturated Si 'dangling' bond (Si·) which can then trap a hole from the Si channel valence band during device operation. (Note: to passivate the generated dangling bond, a second hydrogen atom would need to reach the same site.)

Interestingly, hydroxyl-E' defects are expected to exist also in high-quality SiO_2 layers grown at elevated temperatures. But why do these defects form in larger densities in SiO_2 layers grown at reduced temperatures, becoming the showstopper for NBTI reliability? Following this reasoning, a reduced oxidation temperature limits the relaxation of mechanical strain which naturally builds up at the Si/SiO_2 interface. This results in a larger presence of stretched Si-O bonds, i.e., the precursors of the detrimental hole traps. This hypothesis well matches the experimental observation of NBTI reliability starting to improve only when the oxide is grown at or exposed to temperatures in excess of 700°C. This is the same temperature range reported as required to initiate interface strain relaxation.

Passivating the defects at low temperature with atomic hydrogen: a breakthrough result

The good news: In an earlier theoretical study carried out by collaborators at Vienna University of Technology, it was suggested that hydrogen may be used to passivate the Si dangling bonds at the hydroxyl-E' centers, similarly to the Si dangling bonds present at the Si crystal surface (referred to as Pb centers). The 'straightforward' way would be to perform anneals in a molecular-hydrogen-containing gas ambient, which are indeed among the standard process steps in semiconductor manufacturing. But there is one problem: according to this theoretical study, passivation with molecular

hydrogen requires a sizable energy expenditure (an energy barrier >0.65eV is calculated). In practice, this means that elevated anneal temperatures are required—which is not an option for some novel integration concepts.

We have therefore investigated the idea of supplying excess atomic hydrogen (H* radicals) to SiO_2 right after oxidation, in order to enhance the passivation of the Si dangling bonds at the hydroxyl-E' centers, through a reaction which is expected to be energetically favorable. For the H* exposure, we developed a specific remote (downstream) plasma process operating on an 300mm industry compliant ashing tool. The impact of the treatment exceeded expectations. A substantial improvement in NBTI was observed after exposures at a temperature as low as 100°C: exposing a 600°C-grown SiO_2 interfacial layer to H* for ten minutes yielded an SiO_2 quality already comparable to, or actually slightly better than, a 900°C-grown reference SiO_2 layer. By increasing the exposure temperature to 300°C—which is still far below the set 600°C limit—the oxide quality clearly outperformed that of the 900°C reference layer. By studying the kinetics of the H* passivating reaction with various exposure times and temperatures, an activation energy as low as 0.21eV was estimated, confirming the suitability of the H* treatment for low thermal budget fabrication flows.

It should be noted that the gate stack formation—after treatment with either a high-temperature 'reliability anneal' or with the low-temperature atomic hydrogen exposure—needs to be finalized with a standard sintering step. This is an extra annealing step in a molecular-hydrogen-containing gas ambient at 400-450°C, which is needed to passivate the Si dangling bonds (Pb centers) that remain at the Si crystal surface after oxidation. These dangling bonds have been extensively studied in literature and should not be confused with the Si dangling bonds that reside within the SiO_2 layer, which are the focus of this work as discussed above.

Positive impact on the threshold voltage tuning

A positive side effect observed during the study is that the treatment not only reduces the density of hole traps, but also increases the effective work function of the gate stack. This is ascribed to a concomitant beneficial reduction of the positive fixed charge in the oxide, possibly related to the (upper tail) of the hydroxyl-E' defect band being passivated by the treatment. The effective work function is a critical parameter as it determines the lowest p-type device threshold voltage which can be obtained. The ability to achieve a lower device threshold voltage potentially enables high performance operation at lower voltages.

The defect formation and passivation mechanism

Our team performed additional experiments, in the first place to demonstrate the generality of the defect formation/passivation process. A SiO_2 layer grown at 600°C was passivated by H* before being subjected to a re-oxidation step at a lower temperature (450°C). This flow resulted in a very poor NBTI reliability as oxidation defects could form again, and in even larger density due to the lower (re-)oxidation temperature. However, these newly formed defects could be passivated by performing an additional exposure to atomic hydrogen.

Furthermore, the treatment was applied on a high-quality SiO_2 layer grown at 900°C, i.e. yielding already a good NBTI reliability: an even better robustness was achieved after the H* exposure. These complementary experiments confirm that, despite the different SiO_2 growth and anneal conditions, the same defect formation and passivation mechanisms are at work. The lower the SiO_2 growth temperature, the larger the formed density of hole traps, which can be in any case exhaustively passivated by a properly tuned H* exposure to achieve excellent NBTI reliability.

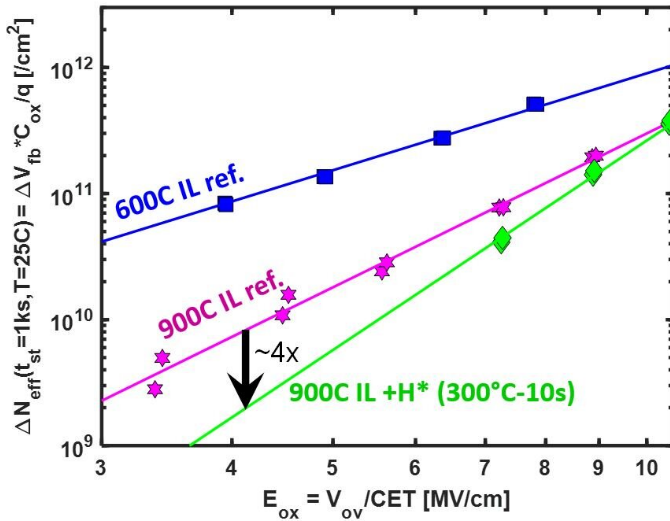

Figure 3 – Impact of a H* treatment on the hole trap defect density within a 900°C grown reference SiO2 layer. Credit: imec

Implications beyond sequential 3-D

We have discussed a unique approach for improving NBTI reliability of pMOS devices fabricated with low thermal budget processes, such as sequential 3-D integration. But the above observations suggest that the approach might be more broadly applicable.

In the standard replacement gate flow, for example, replacing the 'reliability anneal' with an atomic hydrogen treatment could largely simplify the fabrication process flow. The customary 'reliability anneal' not only requires high-temperatures, but often also the deposition of a sacrificial metal gate (typically, titanium-nitride + amorphous Si) in order to control chemical species dynamics during the fast high-temperature anneal and e.g., avoid metal contamination from less thermally stable metal gates. The sacrificial gate is replaced with the final metal gate required to achieve a given device threshold voltage only after the reliability anneal. The equally effective SiO_2 treatment with atomic hydrogen at lower temperatures could allow to omit all the extra process steps related to the deposition and subsequent removal of the sacrificial gate. In addition, the new passivation scheme could become an enabler for future aggressively scaled device architectures, including complementary FET (or CFET) or gate-all-around nanosheet and forksheet transistors, where an extremely tight wire-to-wire pitch might prevent the deposition of a (relatively thick) sacrificial gate for the 'reliability anneal' step.

More information: "Atomic hydrogen exposure to enable high-quality low-temperature SiO2 with excellent pMOS NBTI reliability compatible with 3D sequential tier stacking." 2020 IEDM. ieee-iedm.org/wp-content/uploads/2020/11/20-ap.pdf

Provided by IMEC

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