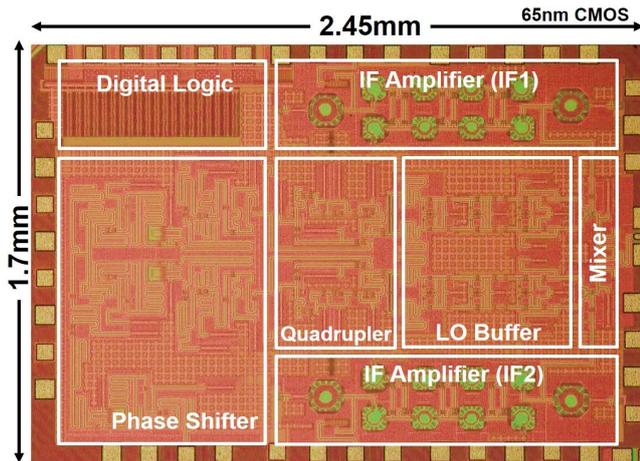


Pushed to the limit: A CMOS-based transceiver for beyond 5G applications at 300 GHz

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amplification becomes considerably difficult. Although a few CMOS-based transceivers for 300 GHz have been proposed, they either lack enough output [power](#), can only operate in direct line-of-sight conditions, or require a large circuit area to be implemented.

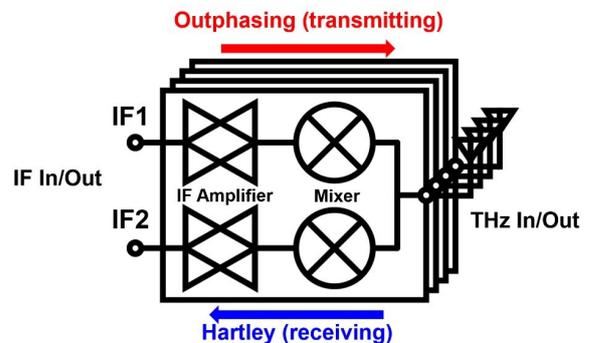
To address these issues, a team of scientists from Tokyo Tech, in collaboration with NTT, proposed an [innovative design](#) for a 300 GHz CMOS-based transceiver (Figure 1). Their work will be presented in the Digests of Technical Papers in the 2021 IEEE ISSCC (International Solid-State Circuits Conference).

Credit: ISSCC 2021

Scientists at Tokyo Institute of Technology (Tokyo Tech) and NTT Corporation (NTT) have developed a novel CMOS-based transceiver for wireless communications at the 300 GHz band, enabling future beyond-5G applications. Their design addresses the challenges of operating CMOS technology at its practical limit and represents the first wideband CMOS phased-array system to operate at such elevated frequencies.

Communication at higher frequencies is goal in electronics as researchers attempt to achieve greater data rates that and to take advantage of underused portions of the electromagnetic spectrum. Many applications beyond 5G, as well as the IEEE802.15.3d standard for [wireless communications](#), call for transmitters and receivers capable of operating close to or above 300 GHz.

Current CMOS technology is not entirely suitable for such elevated frequencies. Near 300 GHz,



※LO generation and phase shifters are omitted

Credit: ISSCC 2021

One of the key features of the proposed design is that it is bidirectional; a great portion of the circuit, including the mixer, antennas and local oscillator, is shared between the receiver and the transmitter (Figure 2). This means the overall circuit complexity and the total circuit area required are much lower than in unidirectional implementations.

Another important aspect is the use of four antennas in a phased array configuration. Existing solutions for 300 GHz CMOS transmitters use a single radiating element, which limits the antenna gain and the system's output power. An additional advantage is the beamforming capability of phased arrays, which allows the device to adjust the relative phases of the antenna signals to create a combined radiation pattern with custom directionality. The antennas used are stacked Vivaldi antennas, which can be etched directly onto PCBs, making them easy to fabricate.

Provided by Tokyo Institute of Technology

The proposed transceiver uses a subharmonic mixer, which is compatible with a bidirectional operation and requires a local oscillator with a comparatively lower frequency. However, this type of mixing results in low output power, which led the team to resort to an old yet functional technique to boost it. Professor Kenichi Okada from Tokyo Tech, who led the study, explains: "Outphasing is a method generally used to improve the efficiency of power amplifiers by enabling their operation at output powers close to the point where they no longer behave linearly—that is, without distortion. In our work, we used this approach to increase the transmitted output power by operating the mixers at their saturated output power." Another notable feature of the new transceiver is its excellent cancelation of local oscillator feedthrough (a "leakage" from the local oscillator through the mixer and onto the output) and image frequency (a common type of interference for the method of reception used).

The entire transceiver was implemented in an area as small as 4.17 mm². It achieved maximum rates of 26 Gbaud for transmission and 18 Gbaud for reception, outclassing most state-of-the-art solutions. Excited about the results, Okada says, "Our work demonstrates the first implementation of a wideband CMOS phased-array system that operates at frequencies higher than 200 GHz."

More information: A 300GHz-Band Phased-Array Transceiver Using Bi-Directional Outphasing and Hartley Architecture in 65nm CMOS, 2021 IEEE International Solid-State Circuits Conference (ISSCC 2021) [isscc.org/](https://www.isscc.org/)

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