Innovative transmitter IC architecture enables >80GHz analog output bandwidth

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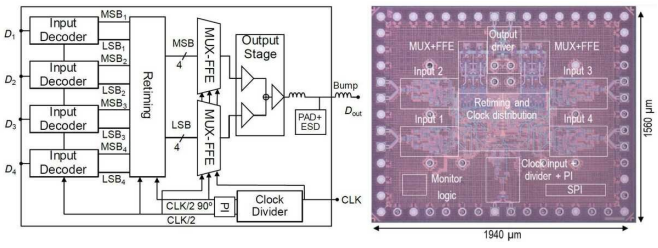


(Left) Block diagram and (right) die micrography of the 4:1 PAM-4 serializer chip with mixed-signal FFE, as presented at 2021 CICC. Credit: IMEC

The growing popularity of data-intensive applications, such as cloud services, video streaming, high-performance computing and 5G, poses ever-increasing demands on optical communication networks within data centers. Here, the most performant optical links operate at speeds up to 400Gb/s, using for example 4 x 100Gb/s channels. Data center operators are however forecasting a need for terabit/s capable optical transceivers within a few years from now. In parallel to this evolution, co-packaged paradigms are emerging to help optical switches cope with the massive bandwidth density at their input—soon reaching 100 terabit/s. In these co-packaged optics, Si photonics transceivers are tightly integrated with the high-speed electronic circuits.

Beyond 100GBaud signaling rates

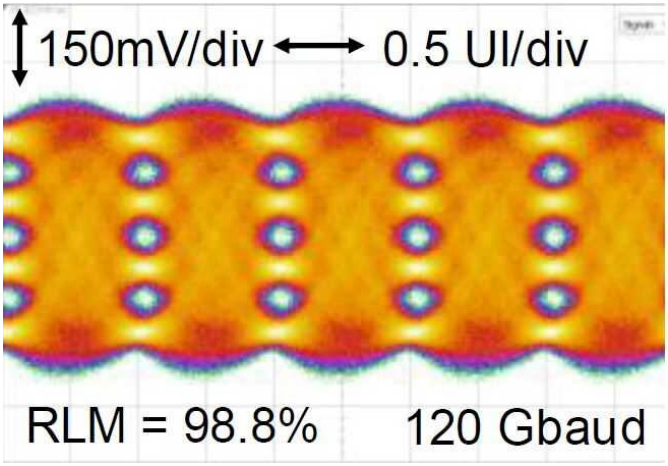
One option to realize terabit/s class optical transceivers is to push the signaling rates well beyond 100Gbaud—the baud rate being the number of symbols that are transmitted per second. On the electronics side, such rates may be beyond the capabilities of even the most advanced CMOS nodes (such as FinFETs), especially in terms of achievable analog bandwidth. Till now, >100Gbaud speeds have been mostly the domain of e.g. InP technologies. Their smaller wafer sizes and reduced capability to integrate more complex functionality makes scaling in such processes challenging. While imec is now pursuing III-V on CMOS processes as a solution in the medium to long term, on the short term, integration of novel circuit architectures in SiGe BiCMOS can be a solution to achieve beyond 100Gbaud operation.

Scientists from imec-IDLab have now come up with a novel transmitter architecture that has key building blocks fabricated in a mainstream SiGe BiCMOS process. Peter Ossieur: "The resulting IC decodes 4x 30Gbaud PAM-4 (or 4x 60Gb/s NRZ) streams, and simultaneously multiplexes and equalizes these streams into a 120Gbaud PAM-4 signal with >80GHz bandwidth, 1.2Vpp voltage swing and 2200mW power consumption. Since the 4-level pulse amplitude PAM-4 modulation format involves two bits per symbol (denoted as 00, 01, 10 and 11), this is the equivalent of a 240Gb/s (single lane) transmitter."

Key SiGe BiCMOS components in an innovative architecture

Within the transmitter IC, a multiplexer (MUX) combines multiple low-speed input signals (coming from e.g. a CPU or GPU within the datacenter) into a single full-rate data stream. This stream is subsequently equalized to compensate for any bandwidth losses in the modulator and the channel. The high-speed equalized signal is then used as an input signal for the driver that subsequently feeds the optical modulator.

In traditional transmitter architectures, equalization is performed in the digital domain, by using a digital signal processor (DSP) fabricated in advanced CMOS nodes. The equalized signal is then converted into an analog signal, feeding the driver. When high voltage swings are required, this driver is nowadays fabricated in III/V technology.



PAM-4 eye diagram at 120Gbaud on a flip-chipped sample with the FFE optimized to reach 500mVpp output, compensating around 8dB of loss at 60GHz. Credit: IMEC

Provided by IMEC

Peter Ossieur: "These building blocks will also be crucial for developing novel coherent transceiver concepts, which exploit the phase and polarization of the optical field to further increase the bit rate. The coherent transceivers target optical communication applications where low cost and low energy are critical objectives."

More information: M. Verplaetse et al, A 4-to-1 240 Gb/s PAM-4 MUX with a 7-tap Mixed-Signal FFE in 55nm BiCMOS, *2021 IEEE Custom Integrated Circuits Conference (CICC)* (2021). DOI: 10.1109/CICC51472.2021.9431514

A 120GBaud PAM-4 prototype

In a prototype transmitter IC, four 30 Gbaud PAM-4 input signals are processed to obtain the two components of the PAM-4 signal, i.e., the most and least significant bit (MSB and LSB) signals. The 4xMSB and 4xLSB signals are separately multiplexed and filtered by the 7-tap FFEs. The filtered signals are combined in the output stage to obtain a full-rate 120GBaud PAM-4 signal, feeding the driver. The transmitter chip is flip chipped on a high-speed PCB to allow for electrical evaluation. "The work shows a doubling of the operating rate compared to FinFET solutions and closely matches the speed and power obtained in InP-based solutions," adds Peter Ossieur.

Future work

The >100Gbaud chips allow progression towards a new generation of optical transceivers, that can transmit these signals in either multiple fibers or at multiple wavelengths to achieve the bit rates required for the terabit era. Apart from the building blocks described above, the team is also working on >100Gbaud transimpedance amplifiers and modulator drivers, high sampling rate ADCs and 100GSample/s analog time interleavers.