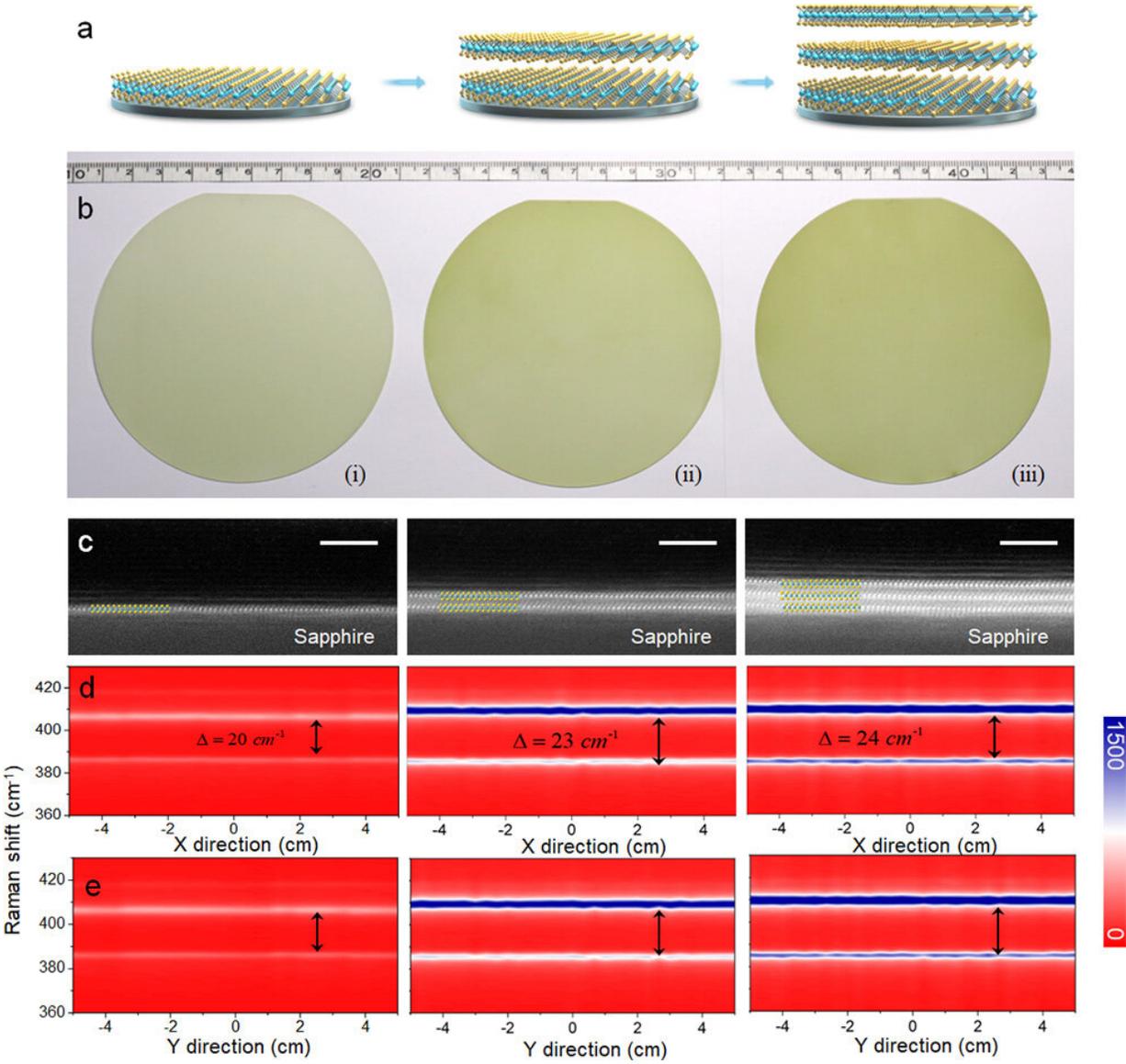


# Epitaxial multilayer MoS2 wafers promise high-performance transistors

June 13 2022, by Zhang Nannan



Layer-by-layer epitaxy of high-quality multilayer MoS2 4-inch wafers. Credit:

Two-dimensional (2D) semiconductors, such as molybdenum disulfide ( $\text{MoS}_2$ ), enable unprecedented opportunities to solve the bottleneck of transistor scaling and to build novel logic circuits with faster speeds, lower power consumption, flexibility and transparency, benefiting from their ultra-thin thickness, dangling-bond-free flat surface and excellent gate controllability.

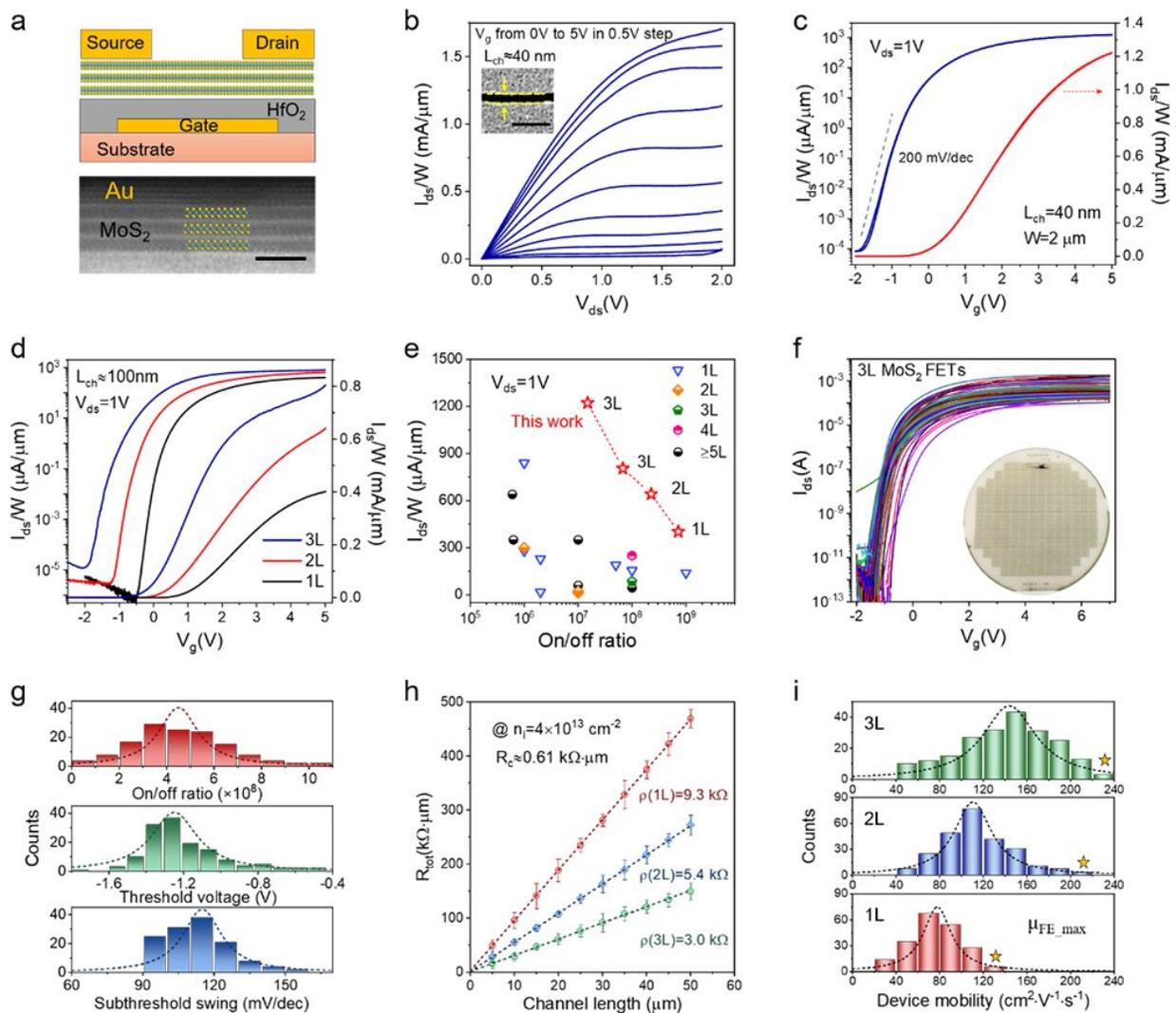
Tremendous efforts have been devoted to exploring the scaled-up potentials of [monolayer](#)  $\text{MoS}_2$ , including both wafer-scale synthesis of high-quality materials and large-area devices. For instance, four-inch wafer-scale monolayer  $\text{MoS}_2$  with large domain sizes (up to  $\sim 300 \mu\text{m}$ ) and record-high electronic quality (average field-effect mobility of  $\sim 80 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ ) has already been demonstrated via van der Waals epitaxial growth.

In terms of a further improvement of the electronic quality of the large-scale monolayer  $\text{MoS}_2$ , structural imperfections should be eliminated as much as possible; however, there is not much space left for monolayer  $\text{MoS}_2$  after ten years of synthesis optimizations in this field. Another key direction is to switch to multilayer  $\text{MoS}_2$ , e.g., bilayers and trilayers, since they have intrinsically higher electronic quality than monolayers and thus are conducive to higher-performance devices and logic circuits. However, due to the fundamental limitation of thermodynamics, it is still a great challenge to realize wafer-scale multilayer  $\text{MoS}_2$  with high-quality and large-scale uniformity.

Recently, Zhang Guangyu's group from the Institute of Physics of the Chinese Academy of Sciences (CAS) has overcome the fundamental limitations of thermodynamics by exploiting the proximity effect of a

sapphire (0001) substrate and achieved, for the first time, the growth of high-quality multilayer MoS<sub>2</sub> four-inch wafers via the layer-by-layer epitaxy process. The epitaxy leads to well-defined stacking orders between adjacent epitaxial layers and offers a delicate control of layer numbers up to six.

Results were published in *National Science Review*.



Bench-mark electronic quality of multilayer MoS<sub>2</sub> field-effect transistors.  
Credit: Institute of Physics

Compared with monolayers, thicker-layer MoS<sub>2</sub> field-effect transistors show significant improvements in device performances. For long-channel devices (channel length of five to 50 μm), the average field-effect mobility at [room temperature](#) can increase from ~80 cm<sup>2</sup>·V<sup>-1</sup>·s<sup>-1</sup> for monolayers to ~110/145 cm<sup>2</sup>·V<sup>-1</sup>·s<sup>-1</sup> for bilayer/trilayer devices, improved by 37.5% / 81.3%.

Considering that, in well-developed [thin-film transistors](#) (TFTs), field-effect mobility is 10–40 cm<sup>2</sup>·V<sup>-1</sup>·s<sup>-1</sup> for indium–gallium–zinc-oxide TFTs and 50–100 cm<sup>2</sup>·V<sup>-1</sup>·s<sup>-1</sup> for low-temperature polycrystalline silicon TFTs, the excellent average field-effect mobility of >100 cm<sup>2</sup>·V<sup>-1</sup>·s<sup>-1</sup> strongly uncovers a great potential of bi- and tri-layer MoS<sub>2</sub> films for high-performance TFT applications.

In addition, for trilayer MoS<sub>2</sub> field-effect transistors, the highest room temperature mobility can reach up to 234.7 cm<sup>2</sup>·V<sup>-1</sup>·s<sup>-1</sup>, setting a new mobility record for devices based on 2D transition-metal sulfide semiconductors.

For devices with a channel length of 100 nm, the [current density](#) (V<sub>ds</sub>=1 V) is increased from 0.4 mA·μm<sup>-1</sup> for monolayer to 0.64/0.81 mA·μm<sup>-1</sup> for bilayer/trilayer, showing an enhancement factor of 60% / 102.5%. Remarkably, for 40 nm short-channel devices, a record-high on-current densities of 1.70/1.22/0.94 mA/μm at V<sub>ds</sub>=2/1/0.65 V, as well as a high on/off ratio exceeding 10<sup>7</sup>, are achieved in trilayer MoS<sub>2</sub> field-effect transistors.

Such high on-current density of trilayer MoS<sub>2</sub> devices outperforms the previous state-of-the-art MoS<sub>2</sub> transistors and also exceeds the target of high-performance logic transistors from the International Roadmap for Devices and Systems 2024, moving a step closer to practical applications

of 2D MoS<sub>2</sub> in electronics and logic circuits at sub-five nm nodes.

**More information:** Qinqin Wang et al, Layer-by-layer epitaxy of multilayer MoS<sub>2</sub> wafers, *National Science Review* (2022). [DOI: 10.1093/nsr/nwac077](https://doi.org/10.1093/nsr/nwac077)

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